REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested. Currently, claims 1 and 4-6 are pending in this application.

Rejection Under 35 U.S.C. §103:

Claims 1 and 4 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Applicant admitted prior art and Shimotashiro et al (U.S. '043, hereinafter "Shimotashiro"). Applicant respectfully traverses this rejection.

In order to establish a prima facie case of obviousness, all of the claim limitations must be taught or suggested by the prior art. The combination of Applicant admitted prior art and Shimotashiro fails to teach or suggest all of the claim limitations. For example, the combination fails to teach or suggest "a temperature characteristic compensating circuit connected to a base of said PNP bipolar transistor and canceling a temperature characteristic of said PNP bipolar transistor to keep a collector current of said PNP bipolar transistor constant," as required by independent claim 1. Similarly, the combination fails to teach or suggest "a temperature characteristic compensating circuit for canceling a temperature characteristic of the PNP bipolar transistor to keep a collector current of said PNP bipolar transistor constant, the temperature characteristic compensating circuit including an NPN bipolar transistor having a conductive terminal connected to a base of said PNP bipolar transistor," as required by independent claim 4.

Through the above claimed limitations, a temperature characteristic is compensated for such that the collector current of a PNP transistor connected between the gate and the drain of a transistor performing frequency conversion is kept constant (e.g., regardless of the temperature). This feature is supported by, for example, page 6, line 30 to page 7, line 12 of the originally-filed specification.

In contrast, Shimotashiro discloses a temperature characteristic which is compensated for such that a delay in delay circuit unit 21 is not changed in a temperature-dependent manner. For example, col. 13, lines 8-10 of Shimotashiro states "Accordingly, the analog signals can be changeably delayed in the delay circuit unit 21, independent of the temperatures of constructional elements (emphasis added)." The current of the current source (IO) corresponding to the collector current of transistor Q21 is thus adjusted in order to compensate for the temperature characteristic of the term RC. (See col. 12, line 43 to col. 13, line 10).

Fig. 4 of Shimotashiro discloses a second delay section 33. In this second delay section 33, current I1 of current source I31 is changed to change the emitter resistance of PNP transistor Q31 so that the temperature characteristic of the delay time added by the second delay section 33 is compensated for as described in col. 15, lines 17-23. However, Applicant submits that Shimotashiro fails to teach or suggest a configuration to compensate for the temperature characteristic of the collector current of PNP transistor Q31. The temperature characteristic to be compensated for differ in the present invention and Shimotashiro.

Accordingly, Applicant respectfully submits that claims 1 and 4 are not obvious over the combination of Applicant admitted prior art and Shimotashiro.

New Claims:

New claims 5-6 have been added to provide additional protection for the invention. Applicant submits that new claims 5 and 6 are allowable at least by virtue of their respective dependencies from independent claims 1 and 4. Claim 5 further requires lessening a variation of a collector current of a PNP bipolar transistor in accordance with a temperature characteristic by adjusting a DC voltage applied to a base of the PNP bipolar transistor according to ambient temperature. Claim 6 further requires maintaining a collector current of a PNP bipolar transistor irrespective on an ambient temperature by adjusting a DC voltage applied to a base of the PNP bipolar transistor according to the ambient temperature. These features are supported by, for example, page 6, line 30 to page 7, line 12 of the originally-filed specification. In contrast, Shimotashiro discloses a signal (AC voltage) provided to input terminal 34 and delayed by first delay section 32 being applied to the base of PNP bipolar transistor Q31. (See col. 4, lines 5-13 of Shimotashiro).

Conclusion:

Applicant believes that this entire application is in condition for allowance and respectfully requests a notice to this effect. If the Examiner has any questions or believes that an interview would further prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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